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Circuit For An Active Pixel Sesnsor

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CIRCUIT FOR AN ACTIVE PIXEL SENSOR

BACKGROUND OF THE INVENTION

[1] Digital cameras and other imaging devices typically have an array of devices, such as pixels arranged on a CMOS microchip for capturing and storing images. Each device and its associated circuitry, the combination of which is often called the Active Pixel Sensor (APS), converts the light intensity detected at each pixel location of the image into a voltage signal that can be digitized for storage, reproduction, and manipulation.

[2] **FIG. 1** is a schematic diagram of showing one implementation of a conventional three-transistor APS ***100*** which digitizes one pixel of an image. The number of pixels in an APS ***100*** array determines the resolution of the captured image. A typical APS ***100*** pixel includes three transistors ***120***, ***121***, and ***122***, and a photodiode ***125*** disposed in a silicon area on top of which are disposed multiple metal layers. Multiple metal layers are typically required because the APS ***100*** requires five terminal traces for operation. This is because the width between each APS ***100*** on a conventional CMOS array only typically allows enough space for two terminal traces per metal layer. The five terminal traces include RESET ***110***, PRESET ***111***, V_{dd} ***112***, COLUMN ***113***, and ROW ***114***. Each APS ***100*** also includes a GROUND ***115*** terminal. By using a controller (not shown) to control the signals at each of the control terminals for the APS ***100*** in conjunction with all other contacts associated with other APSs ***100*** (not shown) in a CMOS array, light intensity striking the CMOS array, *i.e.*, an image, may be detected and digitized.

[3] **FIG. 2** is a timing diagram of the conventional operation of the APS ***100*** of **FIG. 1**. The operation of the APS ***100*** includes a reset phase ***200***, an integration phase ***220***,

and a readout phase ***240***. Each of these phases ***200***, ***220***, and ***240*** is described below with respect to the timing diagram.

[4] Before an image is acquired, each APS ***100*** must first be "cleared" during the reset phase ***200***. This is to make sure that all the pixels in the CMOS array (not shown) have the same starting voltage when the photodiode ***125*** begins integrating light. During time period ***201***, the APS ***100*** is in a previous readout phase ***240*** and, thus (as is explained below with respect to the readout phase ***240***), the RESET ***110*** trace is set to a predetermined low voltage level (typically 0 volts) and the ROW ***113*** and PRESET ***111*** traces are set to a predetermined high voltage level (typically 2.5 – 5.0 volts). At ***t2***, the RESET ***110*** trace is raised to a high voltage level so that the transistor ***121*** acts as a closed switch. As such, the voltage at node ***130*** is equal to the voltage at the PRESET ***111*** trace. The voltage at node ***130*** may turn on transistor ***122***, but any current that may flow through transistor ***122*** is inconsequential because any resultant signal on the COLUMN 113 trace will not be sensed until the readout phase 240 as described below. . Next, the PRESET ***111*** trace is dropped to a predetermined low voltage level while the RESET ***110*** trace remains at the high voltage level. Thus, the voltage at node ***130*** becomes low which causes the parasitic capacitance (not shown) associated with the photodiode ***125*** to be discharged. Finally, the PRESET ***111*** trace is brought back to the high voltage level to charge the parasitic capacitance of the photodiode ***125*** to a predetermined starting voltage level to complete the reset phase ***200.***

[5] Next, during the integration phase ***220***, after the photodiode ***125*** is reset, the RESET ***110*** trace is set to a low voltage so that the transistor ***121*** turns off at t3. Now, the photodiode ***125*** is ready for exposure to light from the image to be captured. During predetermined time period ***204***, the photodiode ***125*** is exposed to light. As is known, the

photodiode ***125*** draws a reverse current that is proportional to the intensity of the light that is striking it, and thus, partially or fully discharges the parasitic capacitance.

[6] After the predetermined integration time period ***204***, the readout phase ***240*** begins. The ROW ***114*** trace is brought to a high voltage level at ***t5*** such that the transistor ***120*** becomes a closed switch and transistor ***122*** acts as a source follower. This results in the voltage at node ***130***, which represents the light intensity detected during the integration phase ***220***, biasing the voltage on the COLUMN ***113*** trace to this voltage level minus the V_{GS} drop from the transistor ***122***. The COLUMN ***113*** trace is coupled to a constant current source (not shown) such that the voltage at node ***130*** will translate to a corresponding voltage on the COLUMN ***113*** trace via transistor ***122***. Since the voltage threshold of the transistor ***122*** is or is approximately the same for all transistors ***122*** in other APSs ***100***, the effects of the V_{GS} drops cancel out such that processing circuitry (not shown) determines the intensity of the light at the pixel captured by the APS ***100*** based on the voltage on the COLUMN ***113*** trace.

[7] Each phase described above is repeated for each row of APSs ***100***, *i.e.*, pixels, in a CMOS array during an image capture procedure. Each row is cycled separately and typically done so in a rolling fashion. That is, when the first row transitions from the reset phase to the integration phase the next row begins the reset phase. Therefore, no row of pixels is ever being read while another row of pixels is being read.

[8] One problem with the APSs ***100*** of **FIG. 1** is that each APS ***100*** requires five terminal traces as described above. As a result, at least three layers of metal, in which the traces (here, two per layer) for each pixel are routed, are typically needed for the CMOS array. These layers of metal are typically disposed on top of the active silicon area in which the integration photodiodes diodes ***125*** and the transistors ***120***, ***121***, and ***122*** are formed. Furthermore, these metal layers are typically separated by relatively

thick layers of dielectric for insulation. Consequently, a conventional CMOS array typically includes at least three layers of metal separated by dielectric.

[9] **FIG. 3** is a diagram of an area occupied by an APS 100 in a conventional CMOS array ***300***. The three layers ***310***, ***311***, and ***312*** of metal separated by oxide insulation ***315*** create a cavity ***320*** above each photodiode ***125***. These cavities ***320*** can cause two problems. First, the thicker and more numerous the metal and oxide layers, the more light is blocked from reaching the photodiodes ***125*** in the CMOS array ***300.*** Therefore, as the thickness and number of the metal and oxide layers increases, the sensitivity of the CMOS array ***300*** decreases.

[10] Second, the higher the cavities ***320***, the closer the angle of incidence ***330*** of the incoming light must be to the normal of the CMOS array ***300***to reach the pixel as evidenced by the shaded region ***325***.. Therefore, if the angle of incidence ***330*** is too great, then the photodiodes ***125*** may not capture the image properly. Furthermore, because of space constraints, a corrective optical train to reduce the angle of incidence may be impractical.

[11] Consequently, it would be desirable to reduce the thickness and/or number of metal and oxide layers in a CMOS pixel array

SUMMARY OF THE INVENTION

[12] According to an embodiment of the invention, a pixel circuit includes a silicon substrate having a photodiode that converts light intensity into a voltage signal. The pixel circuit further includes a row trace and a reset trace. The row trace activates a switch for coupling the photodiode to a column trace during readout phase and clears

the voltage at the photodiode during a reset phase. The pixel circuit further includes a voltage supply trace. A pixel circuit with only four traces requires fewer metal layers.

[13] By having fewer metal layers (for example, a first metal layer for a row trace and a reset trace, and a second metal layer for column trace and V_{dd}), light is more readily able to reach the photodiode while an image is being captured. That is, the cavity discussed above for each pixel is less deep because only two layers of metal are present instead of three. Therefore, it is advantageous to have fewer metal layers for the control circuitry associated with each pixel.

[14] Another advantage of having fewer metal layers is the ability to capture light as larger angles of incidence. Because space is limited in applications, such as, for example, digital camera phones, optical correction trains are impractical between the light source and the CMOS pixel array. Thus, the angle of incidence may be wider in a CMOS pixel array having fewer layers of metal as compared to a conventional CMOS pixel array having more layers of metal for control circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

[15] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same become better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[16] **FIG. 1** is a schematic diagram of a conventional three-transistor pixel-capture circuit;

[17] **FIG. 2** is a timing diagram that illustrates the operation of the three-transistor pixel-capture circuit of **FIG. 1**;

[18] **FIG. 3** is a cutaway view of a region of a conventional CMOS pixel array that includes the three-transistor pixel-capture circuit of **FIG. 1**;

[19] **FIG. 4** is a schematic diagram of a three-transistor pixel-capture circuit according to an embodiment of the invention;

[20] **FIG. 5** is a timing diagram of the operation of the three-transistor pixel-capture circuit of **FIG. 4** according to an embodiment of the invention; and

[21] **FIG. 6** is a block diagram of a CMOS array that includes the pixel-capture circuit of **FIG. 4** according to an embodiment of the invention.

DETAILED DESCRIPTION

[22] **FIG. 4** is a schematic diagram of three-transistor APS ***400*** according to an embodiment of the invention. The APS ***400*** is similar to the APS ***100*** of **FIG.1** except that the APS ***400*** includes only four terminal traces instead of five. This reduction in terminal traces allows a reduction in metal and oxide layers in the corresponding pixel array (**FIG. 6**) and thus improves the sensitivity of the array.

[23] The APS ***400*** includes three transistors ***420***, ***421***, and ***422***, and an integration photodiode ***425*** disposed upon an active silicon area (not shown). However, different from the APS ***100*** of **FIG. 1**, only four terminal traces are required for operation. These four traces include RESET ***410***, V_{dd} ***412***, COLUMN ***413***, and ROW ***414***. Each APS ***400*** also includes a GROUND ***415*** terminal. By having only four traces for each APS ***400***, fewer metal layers are required for the traces. In the embodiment shown here, the

APS ***400*** eliminates the PRESET ***111*** trace that was present in the conventional APS ***100*** shown in **FIG. 1**. By combining the clearing function of the PRESET ***111*** trace with the function of the ROW ***414*** trace, only four traces are used for operation.

[24] **FIG. 5** is a timing diagram that illustrates the operation of the APS ***400*** of **FIG. 4**. The operation of the APS 400 includes a reset phase ***500***, an integration phase ***520***, and a readout phase ***540***. Each of these phases ***500***, ***520***, and ***540*** is described below.

[25] Before an image is acquired, the APS ***400*** is cleared during the reset phase ***500***. During time period ***501***, the APS ***400*** is in a previous readout phase ***540*** and, thus, the RESET ***510*** trace is set to a predetermined low voltage level and the ROW ***413*** trace is set to a predetermined high voltage level. At ***t2*** , the RESET ***410*** trace is raised to a high voltage level so that the transistor ***421*** acts as a closed switch such that the voltage at node ***430*** is equal to the voltage at the ROW ***414*** trace. The voltage at node ***430*** may turn on transistor ***422***, and some current may flow through transistor ***422*** because the ROW ***414*** trace, which is also coupled to the gate of transistor ***420,*** is at a high voltage level and the transistor ***420*** is on. However, since the COLUMN ***413*** trace is not being accessed, *i.e.*, this is not the readout phase ***540***, such a voltage on the COLUMN ***413*** trace typically does not adversely affect the operation of the CMOS array.

[26] Next, the ROW ***414*** trace is dropped to a predetermined low voltage level while the RESET ***410*** trace remains at the high voltage level. Thus, the voltage at node ***430*** becomes low to discharge the photodiode ***425***. Then, the ROW ***414*** trace is brought back to the high voltage to charge the parasitic capacitance associated with the photodiode to a predetermined starting voltage level and complete the reset phase ***500.***

[27] Next, during the integration phase ***520***, after the parasitic capacitance associated with the photodiode ***425*** is discharged, the RESET ***410*** trace is set to a low voltage so

that the transistor ***421*** turns off at ***t3***. Now, the photodiode ***425*** is exposed to light during predetermined integration period ***504***.

[28] After the predetermined integration period ***504***, the readout phase ***540*** begins. The ROW ***414*** trace is brought to a high voltage level at ***t5***, such that the transistor ***420*** is turned on and becomes a closed switch and transistor ***422*** acts as a source follower. The predetermined high voltage during the readout phase ***540*** may be the same as during the reset phase, but may vary depending on the current required to turn on transistor ***422***. This results in the voltage at node ***430***, which represents the light intensity detected during the integration phase ***520***, biasing the voltage on the COLUMN ***413*** terminal minus the V_{GS} drop from the transistor ***422***. Again, since the voltage threshold of the transistor ***422*** is or is approximately the same for all transistors ***422*** in other APSs ***400***, the effect of the V_{GS} drop cancels out such that processing circuitry (not shown) determines the intensity of the light at the pixel based on the voltage on the COLUMN ***413*** trace.

[29] Each phase described above is repeated for each row of pixels (APSs ***400***) during an image-capture procedure. Each row is cycled separately and typically done so one after another. That is, after the first row transitions through each of the three above-described phases, the next adjacent row begins with its transition through the phases starting with the reset phase. Therefore, no row of pixels is ever being read while another row of pixels is being read. This is shown in greater detail with respect to **FIG. 6**, described below.

[30] **FIG. 6** shows a block diagram of a system ***600*** that includes a CMOS pixel array ***610*** having several APSs ***400*** of **FIG. 4**, disposed therein. The system ***600*** may be a digital camera, digital camera-phone, or other electronic device utilizing a digital image-capturing apparatus. The system includes a central processing unit (CPU) ***615***

coupled with a bus ***620***. Also coupled with the bus ***620*** is a memory ***625*** for storing digital images captured by the CMOS array ***610***. The CPU ***615*** facilitates an image capture by controlling the CMOS array ***610*** through the bus ***625*** and, once an image is captured, storing of the image in a digital format in the memory ***625***.

[31] The CMOS array ***610*** includes several components for facilitating the capture and digitizing of an image. Each APS ***400*** in the CMOS array ***610*** is coupled to ROW control circuitry ***650*** and to COLUMN control circuitry ***660*** which facilitate the control signals described above with respect to **FIGs. 4** and **5**. More specifically, each APS ***400*** in a single row of pixels is coupled to a dedicated ROW (***414*** of **FIG. 4**) control line and a dedicated RESET (***410*** of **FIG. 4**) control line via connection ***651***. Additionally, each APS ***400*** in a single column is coupled to a dedicated COLUMN (***413*** of **FIG. 4**) control line via connection ***661***. Further, each APS ***400*** in the CMOS array ***610*** is coupled to V_{dd} ***611*** and GROUND ***612*** (individual connection not shown).

[32] As was described previously with respect to **FIG. 5**, each row of the CMOS array ***610*** is read separately. For example, each pixel in the first row ***652*** starts the image capture procedure, *i.e.*, reset ***500***, integration ***520***, and readout ***540***, prior to the next row ***653*** starting the same image capture procedure. During the readout phase ***540***, the voltage on the COLUMN ***413*** trace at each APS 400 in the first row is read by the column control circuitry ***660*** and sent to a multiplexor ***670***. The multiplexor combines each COLUMN ***413*** trace voltage signal into a single multiplexed signal which represents the voltage signal, *i.e.*, pixel, captured at each photodiode ***425*** of each pixel in the particular row being read. After an amplification stage ***680***, this signal is converted into a digital signal via an analog-to-digital converter ***690*** before being communicated to the bus ***620***. The CPU ***615*** then facilitates the storage in the memory ***625*** of the digital signal in conjunction with the next digital signal representing

the next row and so on. This procedure is repeated for each row in the CMOS array ***610*** until each row has been read and a complete digital image has been stored in the memory ***625***.

[33] The preceding discussion is presented to enable a person skilled in the art to make and use the invention. The general principles described herein may be applied to embodiments and applications other than those detailed below without departing from the spirit and scope of the present invention. The present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed or suggested herein.